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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/632,872	08/01/2003	Joseph H. End III	TN302	4647

7590 03/23/2006

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EXAMINER

CHERY, MARDOCHEE

ART UNIT	PAPER NUMBER
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2188

DATE MAILED: 03/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/632,872	Applicant(s) END, JOSEPH H.	
	Examiner Mardochee Chery	Art Unit 2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 01 August 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-22 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date: _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>8/1/03</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Objections

1.
 - a. Claim 7 is objected to because of the following informalities: in line 3 "ones of" should be deleted.
 - b. Claim 13 is objected to because of the following informalities: in line 5 "ones of" should be deleted.
- Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.
3. Claim 8 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. In line 3 the claim recites "first and second memory banks are not equal". However, the specification does not describe how two memory banks are made equal or not equal, although it is known in the art to compare addresses of two memory banks and determine whether they are equal.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nystuen (2004/0088472) in view of Shiozaki et al. (4,683,533).

As per claim 1, Nystuen discloses a memory controller for managing memory requests from a plurality of requesters to a plurality of memory banks, the memory controller comprising: an arbiter configured to receive the memory requests from the plurality of requesters, the arbiter assigning a first memory request to a first processing path and a second memory request to a second processing path responsive to the memory banks requested by the received and assigned memory requests [Fig. 3; par. 3]; a first path controller coupled to the arbiter and the plurality of memory banks, the first path controller configured to process the first memory request in the first processing path to activate a first memory bank associated with the first memory request [Figs. 3 and 5; pars. 28-30]; a second path controller coupled to the arbiter and the plurality of memory banks, the second path controller configured to process the second memory request in the second processing path to activate a second memory bank associated with the second memory request while the first memory bank is active [Figs. 1 and 3;

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pars. 23-28]; and a synchronizer coupled between the first path controller and the second path controller for synchronizing the first and second path controllers such that the first and second memory requests processed by the first and second path controllers, respectively, do not conflict [col. 1, ll 33-38; col. 2, ll 17-23 and col. 3, ll 25-36];

However Nystuen does not specifically teach a second path controller configured to process the second memory request in the second processing path as required by the claim.

Shiozaki discloses a second path controller configured to process the second memory request in the second processing path [col.4, lines 27-29; col.1, lines 8-15; col.3, lines 31-36; col.1, lines 25-27; col.2, lines 39-42] to prevent a conflict from taking place during an update operation (col. 2, ll 17-23).

Since the technology for implementing a memory controller with a second path controller configured to process the second memory request in the second processing path was well known as evidenced by Shiozaki, an artisan would have been motivated to implement this feature in the system of Nystuen in order to avoid conflict during an update operation. Thus, it would have been obvious to one of ordinary skill in the art at the time of invention by Applicant to modify the system of Nystuen to include a second path controller configured to process the second memory request in the second

processing path because this would have prevented conflict from taking place during an update operation (col. 2, ll 17-23) as taught by Shiozaki.

As per claim 2, Shiozaki discloses the arbiter, the first path controller, the second path controller, and the synchronizer are implemented as a single field programmable gate array [col.4, lines 27-29; col.1, lines 8-15; col.3, lines 31-36; col.1, lines 25-27].

As per claim 3, Nystuen discloses the arbiter, the first path controller, the second path controller, and the synchronizer are configured for use with an SDRAM memory device comprising the first and second memory banks [Figs. 3 and 5].

As per claim 4, Nystuen discloses a first path timing controller that controls the first path circuitry and activates the first memory bank associated with the first memory request [Figs. 8-9]; and address and data multiplexers that multiplex addresses and data associated with the first memory request for interfacing with the memory banks [Fig. 5; MUX 520]; a second path timing controller that controls the second path circuitry and activates the second memory bank associated with the second memory request [Figs. 8-9]; and the address and data multiplexers that multiplex addresses and data associated with the first memory request, the address and data multiplexers further multiplexing addresses and data associated with the second memory request for interfacing with the memory banks [Fig. 5; MUX 520].

However, Nystuen does not specifically teach the first path controller comprises at least : first path circuitry that passes addresses and data associated with the first memory request ; and wherein the second path controller comprises at least: second path circuitry that passes addresses and data associated with the second memory request as required by the claim.

Shiozaki discloses the first path controller comprises at least : first path circuitry that passes addresses and data associated with the first memory request [Fig. 1; col. 2, ll 1-5 and ll 12-28]; and wherein the second path controller comprises at least: second path circuitry that passes addresses and data associated with the second memory request [Fig. 1; col. 1, ll 6-15 and ll 51-60] to prevent a conflict from taking place during an update operation (col. 2, ll 17-23).

Since the technology for implementing a memory controller with a first path circuitry that passes addresses and data associated with the first memory request and a second path circuitry that passes addresses and data associated with the second memory request was well known as evidenced by Shiozaki, an artisan would have been motivated to implement this feature in the system of Nystuen in order to avoid conflict during an update operation. Thus, it would have been obvious to one of ordinary skill in the art at the time of invention by Applicant to modify the system of Nystuen to include a first path circuitry that passes addresses and data associated with the first memory request and a second path circuitry that passes addresses and data associated with the

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second memory request because this would have prevented conflict from taking place during an update operation (col. 2, ll 17-23) as taught by Shiozaki.

As per claim 5, Shiozaki discloses the synchronizer comprises: delay circuits coupled between the first and second path controllers to set delay values therebetween to adjust the timing of the first and second path controllers during processing of the first and second memory requests responsive to the first and second memory requests [col. 2, ll 48-57 and col. 3, ll 18-24].

As per claim 6, Nystuen discloses the first path controller is further configured to initialize and refresh the plurality of memory banks [par. 73].

As per claim 8, Nystuen discloses the arbiter assigns the second memory request to the second path controller when the first path controller is active if the first and second memory banks are not equal [Fig. 3].

As per claim 9, the rationale in the rejection of claim 1 is herein incorporated.

As per claim 10, the rationale in the rejection of claim 4 is herein incorporated.

As per claim 11, the rationale in the rejection of claim 5 is herein incorporated.

As per claim 12, Nystuen discloses initializing the plurality of memory banks using the first processing path [par. 50].

As per claim 13, Nystuen discloses receiving the memory requests from the plurality of memory requesters during a current arbitration cycle [par. 30]; comparing the plurality of memory requesters to a grant history register identifying the plurality of memory requesters that have had previous memory requests granted during the current cycle [pars. 45- 47]; identifying the first memory request by a first memory requester from the plurality of memory requesters not on the grant history register and not having a current request in the second processing path using fixed priority logic [pars. 30 and 34]; and adding the first memory requester to the grant history register [par. 32].

As per claim 14 the rationale in the rejection of claim 8 is herein incorporated.

As per claim 15 the rationale in the rejection of claim 9 is herein incorporated.

As per claim 16, Nystuen discloses means for combining the first and second memory requests for accessing the plurality of memory banks, wherein the processing means comprises generating a read command or a write command in each of the first and second processing paths and wherein the commands are concatenated by synchronizing and combining means [Fig. 3; pars. 28 and 32].

As per claim 17, the rationale in the rejection of claim 13 is herein incorporated.

As per claim 18, Nystuen discloses identifying from the plurality of memory requesters not on the grant register a lowest memory requester having a lowest value among the plurality of memory requesters not on the grant history register for assignment to one of the at least one controller [pars. 45-47].

As per claim 21, the rationale in the rejection of claim 13 is herein incorporated.

As per claim 22, Nystuen discloses the arbiter and the at least one path controller are implemented in a field programmable gate array [par. 31].

Allowable Subject Matter

6. Claims 7, 19 and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

7. When responding to the office action, Applicant is advised to clearly point out the patentable novelty that he or she thinks the claims present in view of the state of the art disclosed by references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. 1.111(c).

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mardochee Chery whose telephone number is (571) 272-4246. The examiner can normally be reached on 8:30A-5:00P.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Manonama Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

March 17, 2006



Mardochee Chery
Examiner
AU 2188


MANO PADMANABHAN 3/17/06
SUPERVISORY PATENT EXAMINER